

Features

- Uses CRM(CQ) advanced SkyMOS2 technology
- Extremely low on-resistance $R_{DS(on)}$
- Excellent $Q_g \times R_{DS(on)}$ product(FOM)
- AEC-Q101 Qualified
- MSL1 up to 260°C peak reflow

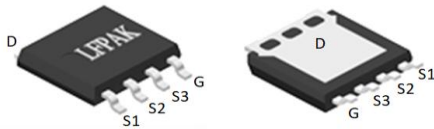
Applications

- Motor control and drive
- Battery management
- UPS (Uninterruptible Power Supplies)

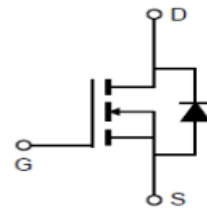
Product Summary

V_{DS}	60V
$R_{DS(on)}@10V$ typ	4.5mΩ
I_D	90A

100% DVDS Tested
100% Avalanche Tested



CRSY045N06L2Q



Package Marking and Ordering Information

Part #	Marking	Package	Packing	Reel Size	Tape Width	Qty
CRSY045N06L2Q	045N06L2Q	LPAK5*6	Tape&reel	N/A	N/A	4000pcs

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	60	V
Continuous drain current $T_C = 25^\circ\text{C}$ (Silicon limit) $T_C = 100^\circ\text{C}$ (Silicon limit)	I_D	90 66	A
Pulsed drain current ($T_C = 25^\circ\text{C}$, t_p limited by T_{jmax})	$I_{D \text{ pulse}}$	372	A
Avalanche energy, single pulse ($L=0.3\text{mH}$, $R_g=25\Omega$) ^[1]	E_{AS}	109	mJ
Gate-Source voltage	V_{GS}	± 20	V
Power dissipation ($T_C = 25^\circ\text{C}$)	P_{tot}	94	W
Operating junction and storage temperature	T_j, T_{stg}	-55...+175	$^\circ\text{C}$
Soldering temperature, wave soldering only allowed at leads (1.6mm from case for 10s)	T_{sold}	260	$^\circ\text{C}$

Notes:1.EAS was tested at $T_j = 25^\circ\text{C}$, $L = 0.3\text{mH}$, $I_{AS} = 27\text{A}$, $V_{gs}=10\text{V}$.

Thermal Resistance

Parameter	Symbol	Max	Unit
Thermal resistance, junction – case.	R_{thJC}	1.6	$^\circ\text{C/W}$
Thermal resistance, junction – ambient(min. footprint)	R_{thJA}	62	
Thermal resistance, junction – plastic case	R_{thj-pc}	21	

Electrical Characteristic (at T_j = 25 °C, unless otherwise specified)

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Static Characteristic						
Drain-source breakdown voltage	BV _{DSS}	60	-	-	V	V _{GS} =0V, I _D =250uA
		60	-	-	V	V _{GS} =0V, I _D =1mA
Gate threshold voltage	V _{GS(th)}	1.2	-	2.2	V	V _{DS} =V _{GS} , I _D =250uA
Zero gate voltage drain current	I _{DSS}	-	-	1	μA	V _{DS} =60V, V _{GS} =0V T _j =25°C
		-	-	100		T _j =125°C
Gate-source leakage current	I _{GSS}	-	-	±100	nA	V _{GS} =±20V, V _{DS} =0V
Drain-source on-state resistance	R _{DS(on)}	-	4.5	6.0	mΩ	V _{GS} =10V, I _D =40A
		-	6.3	10.0		V _{GS} =4.5V, I _D =32A
Transconductance	g _{fs}	55	110	220	S	V _{DS} =5V, I _D =40A

Dynamic Characteristic

Input Capacitance	C _{iss}	880	1760	3520	pF	V _{GS} =0V, V _{DS} =30V, f=1MHz
Output Capacitance	C _{oss}	230	460	920		
Reverse Transfer Capacitance	C _{rss}	-	30	120		
Gate Total Charge	Q _G	15	30	60	nC	V _{GS} =10V, V _{DS} =30V, I _D =40A, f=1MHz
Gate-Source charge	Q _{gs}	-	9	20		
Gate-Drain charge	Q _{gd}	-	5	25		
Turn-on delay time	t _{d(on)}	-	11	20	ns	V _{GS} =10V, V _{DD} =30V, R _{G_ext} =3Ω, I _D =40A
Rise time	t _r	60	75	145		
Turn-off delay time	t _{d(off)}	-	23	46		
Fall time	t _f	-	98	196		
Gate resistance	R _G	-	0.8	3	Ω	V _{GS} =0V, V _{DS} =0V, f=1MHz

Body Diode Characteristic

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Body Diode Forward Voltage	V _{SD}	-	0.9	1.4	V	V _{GS} =0V, I _{SD} =40A
Body Diode Reverse Recovery Time	t _{rr}	10	25	50	ns	I _F =40A, dI/dt=100A/μs
Body Diode Reverse Recovery Charge	Q _{rr}	-	21	42	nC	

Typical Performance Characteristics

Fig 1: Output Characteristics

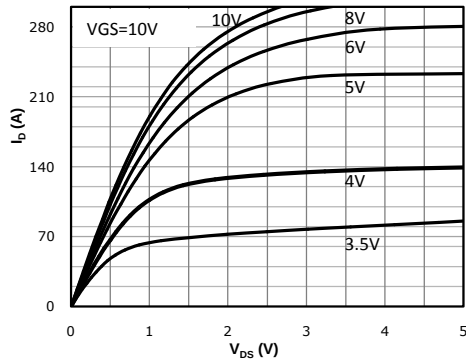
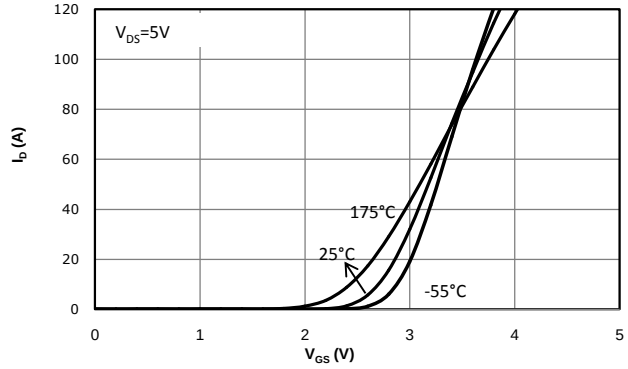


Fig 2: Transfer Characteristics



3: Rds(on) vs Drain Current and Gate Voltage

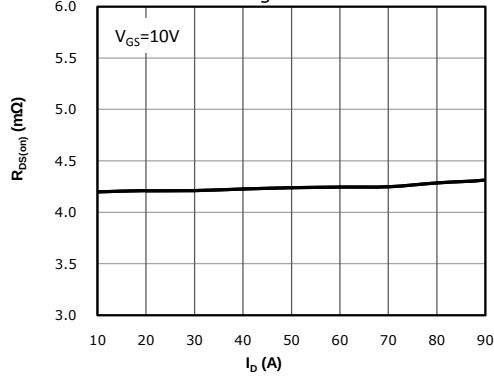


Fig 4: Rds(on) vs Gate Voltage

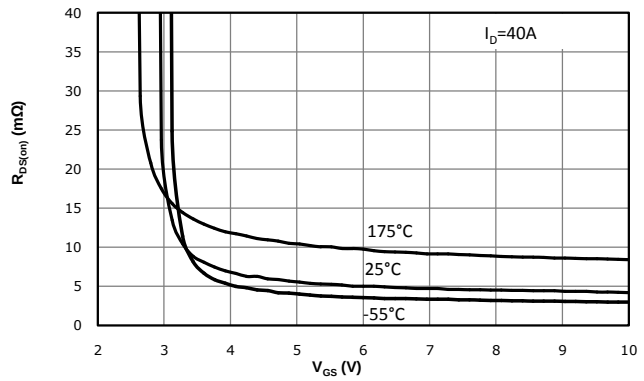


Fig 5: Rds(on) vs. Temperature

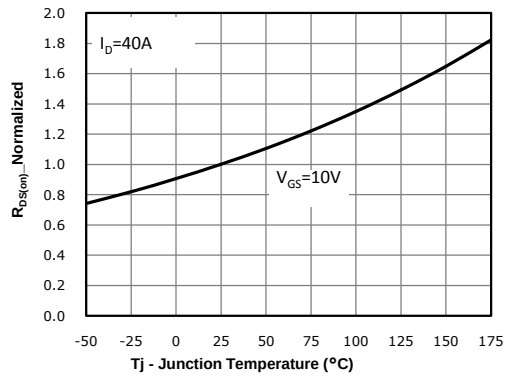


Fig 6: Vgs(th) vs. Temperature

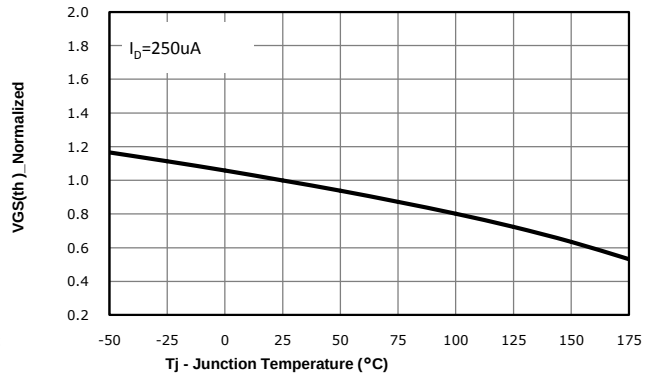


Fig 7: BVds vs. Temperature

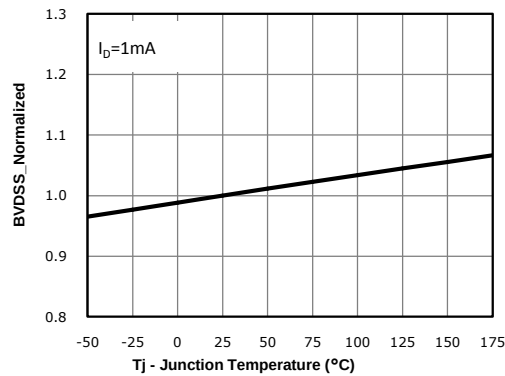


Fig 8: Capacitance Characteristics

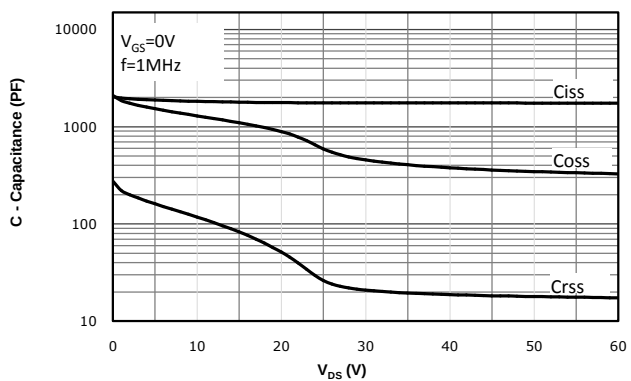


Fig 9: Gate Charge Characteristics

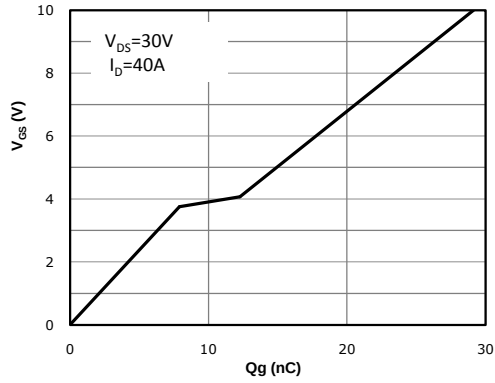


Fig 10: Body-diode Forward Characteristics

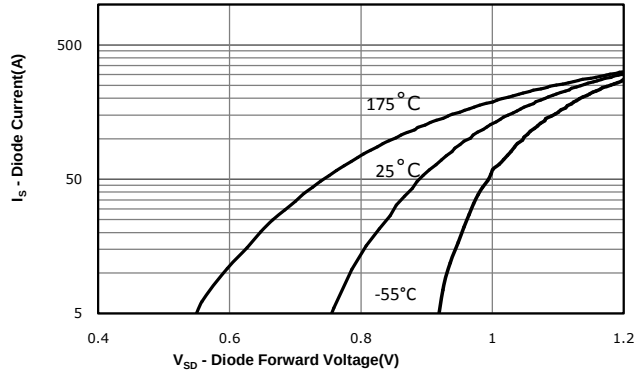


Fig 11: Power Dissipation

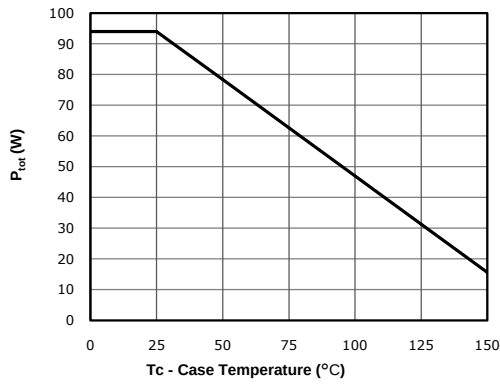


Fig 12: Drain Current Derating

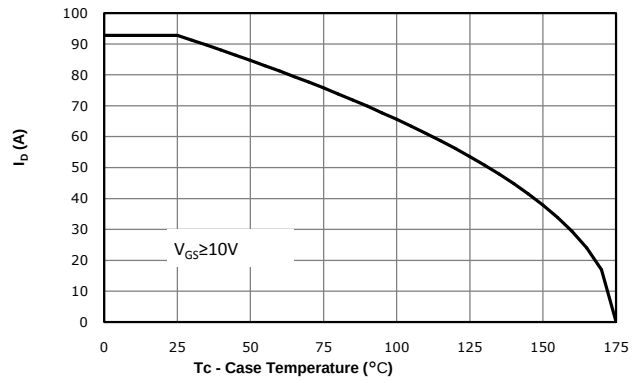


Fig 13: Safe Operating Area

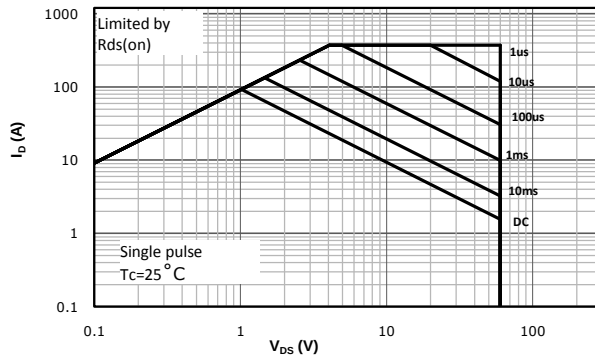
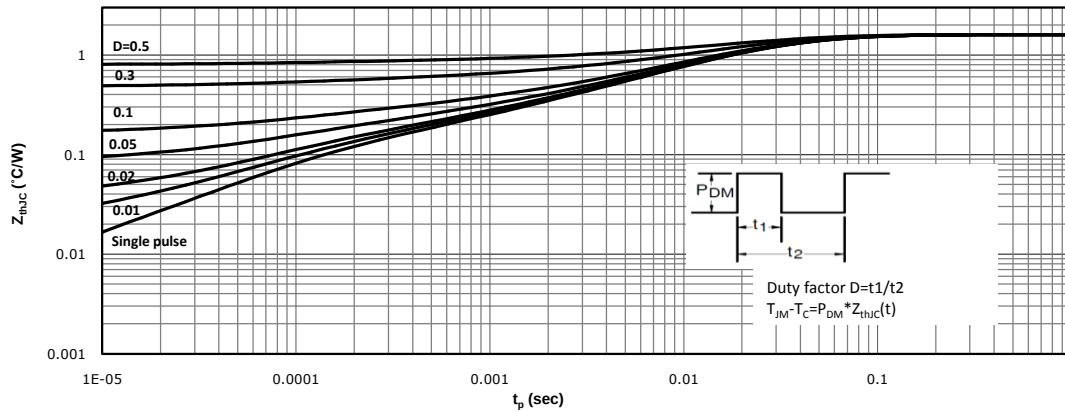
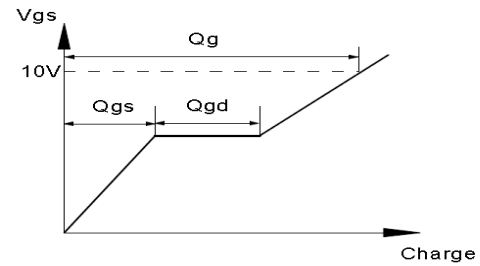
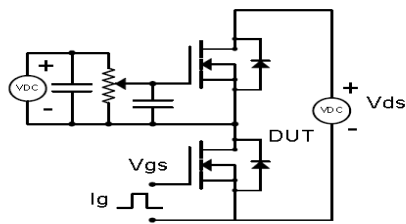


Fig 14: Max. Transient Thermal Impedance

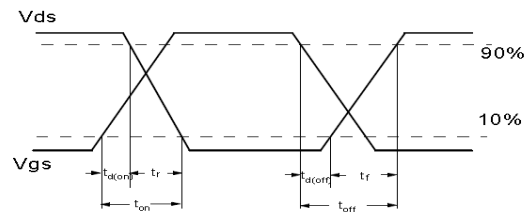
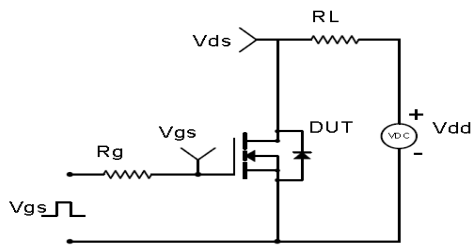


Test Circuit & Waveform

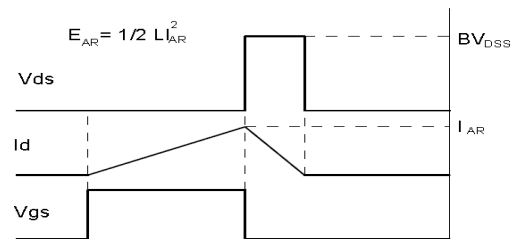
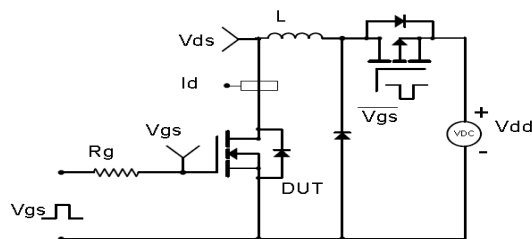
Gate Charge Test Circuit & Waveform



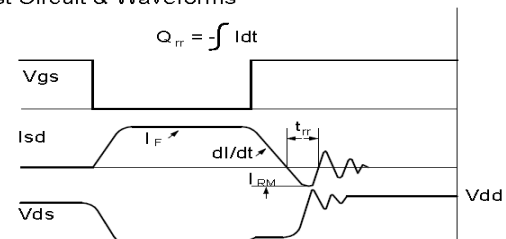
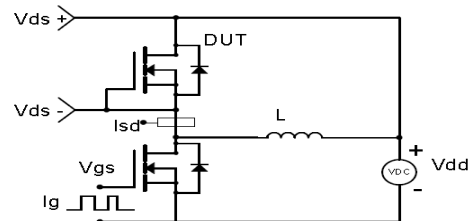
Resistive Switching Test Circuit & Waveforms



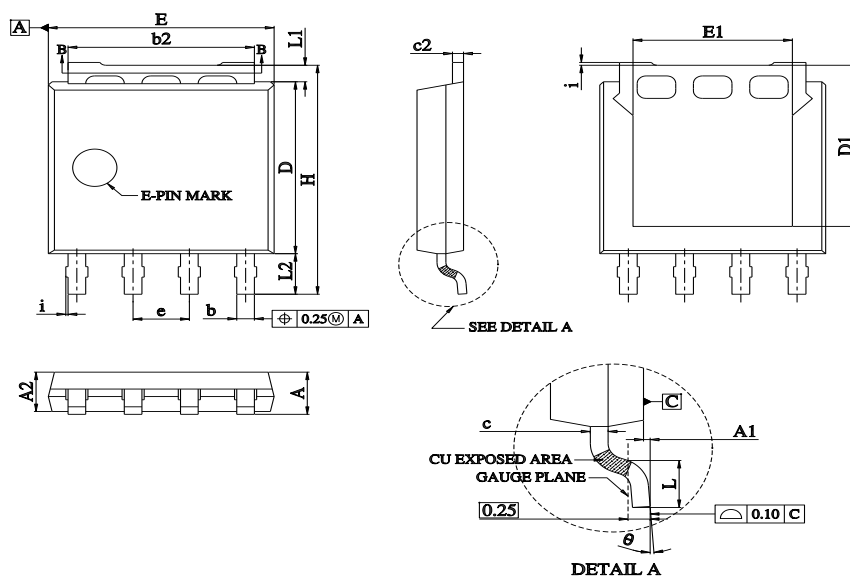
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

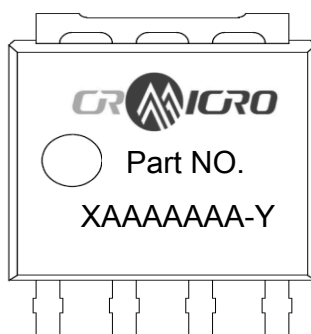


Package Outline: LFPAK5*6



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.00	1.20	0.039	0.047
A1	0.00	0.15	0.000	0.006
A2	0.95	1.15	0.037	0.045
b	0.32	0.50	0.013	0.020
b2	3.80	4.41	0.150	0.174
c	0.17	0.25	0.007	0.010
c2	0.22	0.30	0.009	0.012
D	4.45	4.70	0.175	0.185
D1	--	4.45	--	0.175
E	4.90	5.30	0.193	0.209
E1	3.45	3.75	0.136	0.148
e	1.27 BSC		0.050 BSC	
H	5.95	6.25	0.234	0.246
i	--	0.25	--	0.010
L	0.40	0.85	0.016	0.033
L1	0.27	0.57	0.011	0.022
L2	0.80	1.30	0.031	0.051
θ	0°	8°	0°	8°

Marking



NOTE:
XAAAAAAA-Y□
X —Assembly location code
AAAAAAA —Assembly lot NO.last 7digits
Y —Bin code

Reversion History

Reversion	Date	Major changes
1.0	2023/9/12	Release of preliminary 1.0 version.
2.0	2024/3/14	Change RthJA/Rthj-pc Max.

Disclaimer

CRM reserves the right to change any product or information in this Specification at any time without prior notice.

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