

Features

- CRM(CQ) Super_Junction technology
- Much lower $R_{on} \cdot A$ performance for On-state efficiency
- Better efficiency due to very low FOM

Applications

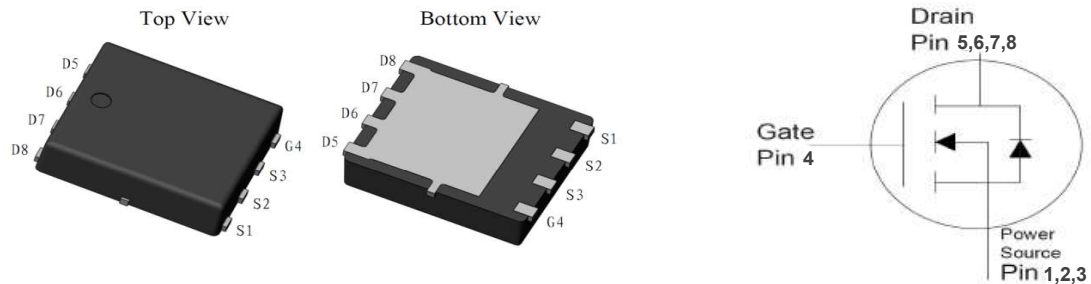
- LED/LCD/PDP TV and monitor Lighting
- Solar/Renewable/UPS-Micro Inverter System
- Charger
- Power Supply

Product Summary

$V_{DS,min}$	650V
$R_{DS(on),typ}$	1.1Ω
I_D	4A

100% DVDS Tested

100% Avalanche Tested



Package Marking and Ordering Information

Part #	Marking	Package	Packing	Reel Size	Tape Width	Qty
CRJM1K2N65G2	1K2N65G2	DFN5*6	Tape&Reel	N/A	N/A	4000/5000pcs

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	650	V
Continuous drain current ¹⁾ $T_C = 25^\circ\text{C}$ $T_C = 100^\circ\text{C}$	I_D	4 2	A
Pulsed drain current ²⁾ ($T_C = 25^\circ\text{C}$, t_p limited by $T_{j,max}$)	$I_{D,pulse}$	15	A
Avalanche energy, single pulse ($L=30\text{mH}$)	E_{AS}	35	mJ
MOSFET dv/dt ruggedness	dv/dt	50	V/ns
Gate-Source voltage	V_{GS}	± 30	V
Power dissipation ($T_C = 25^\circ\text{C}$)	P_{tot}	36	W
Continuous diode forward current ($T_C = 25^\circ\text{C}$)	I_S	4	A
Diode pulse current ²⁾ ($T_C = 25^\circ\text{C}$)	$I_{S,pulse}$	15	A
Recovery diode dv/dt ³⁾	dv/dt	50	V/ns
Operating junction and storage temperature	T_j, T_{stg}	-55...+150	$^\circ\text{C}$

1) Limited by $T_{j,max}$. Maximum Duty Cycle $D = 0.50$

2) Pulse width t_p limited by $T_{j,max}$

3) Identical low side and high side switch with identical R_g

Thermal Resistance

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Thermal resistance, junction – case	R_{thJC}	-	2.47	3.46	°C/W	
Thermal resistance, junction – ambient	R_{thJA}	-	-	56	°C/W	

Electrical Characteristic (at $T_j=25^{\circ}\text{C}$, unless otherwise specified)

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		

Static Characteristic

Drain-source breakdown voltage	BV_{DSS}	650	-	-	V	$V_{GS}=0V, I_D=250\mu A$
Gate threshold voltage	$V_{GS(th)}$	3	-	4	V	$V_{DS}=V_{GS}, I_D=250\mu A$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=650V, V_{GS}=0V$ $T_j=25^{\circ}\text{C}$
		-	1	-		$T_j=150^{\circ}\text{C}$
Gate-source leakage current	I_{GSS}	-	-	± 100	nA	$V_{GS}=\pm 30V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	1.1	1.20	Ω	$V_{GS}=10V, I_D=1.5A$ $T_j=25^{\circ}\text{C}$
		-	2.5	-		$T_j=150^{\circ}\text{C}$
Transconductance	g_{fs}	-	2.9	-	S	$V_{DS}=20V, I_D=1.5A$

Dynamic Characteristic

Input Capacitance	C_{iss}	-	221	-	pF	$V_{GS}=0V, V_{DS}=100V, f=1\text{MHz}$
Output Capacitance	C_{oss}	-	15	-		
Reverse Transfer Capacitance	C_{rss}	-	0.9	-		
Gate Total Charge	Q_g	-	7.9	-	nC	$V_{GS}=10V, V_{DS}=480V, I_D=1.5A$
Gate-Source charge	Q_{gs}	-	1.7	-		
Gate-Drain charge	Q_{gd}	-	3.45	-		
Gate plateau voltage	$V_{plateau}$	-	5.3	-	V	
Turn-on delay time	$t_{d(on)}$	-	12.5	-	ns	$V_{GS}=10V, I_D=1.5A,$ $V_{DS}=400V, R_g=27\Omega$
Rise time	t_r	-	8.6	-		
Turn-off delay time	$t_{d(off)}$	-	36	-		
Fall time	t_f	-	88	-		
Gate resistance	$R_{g,int}$	-	6.2	-	Ω	$f=1\text{MHz}$

Body Diode Characteristic

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Body Diode Forward Voltage	V_{SD}	0.6	0.83	1.1	V	$V_{GS}=0V, I_{SD}=1.5A$
Body Diode Reverse Recovery Time	t_{rr}	-	126	-	ns	$I_{SD}=1.5A$ $di_F/dt=100A/\mu s$
Body Diode Reverse Recovery Charge	Q_{rr}	-	0.7	-	μC	$V_{DS}=100V$

Typical Performance Characteristics

Fig 1. Output Characteristics ($T_J=25^\circ\text{C}$)

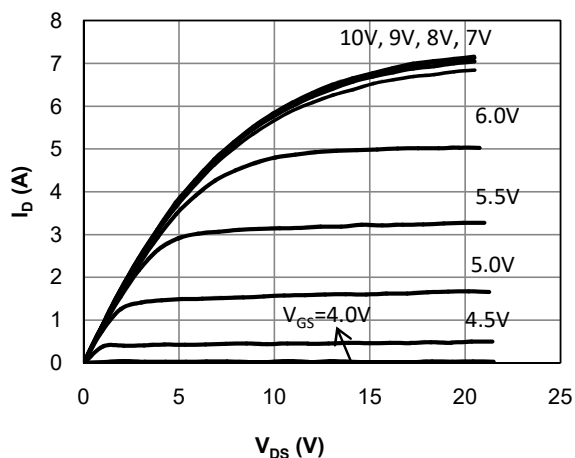


Fig 2. Output Characteristics ($T_J=150^\circ\text{C}$)

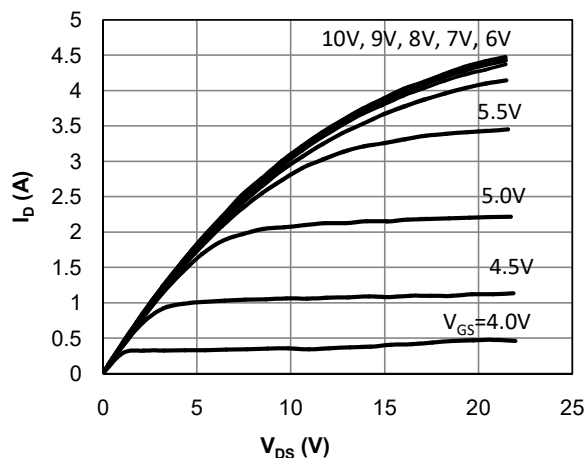


Fig 3: Transfer Characteristics

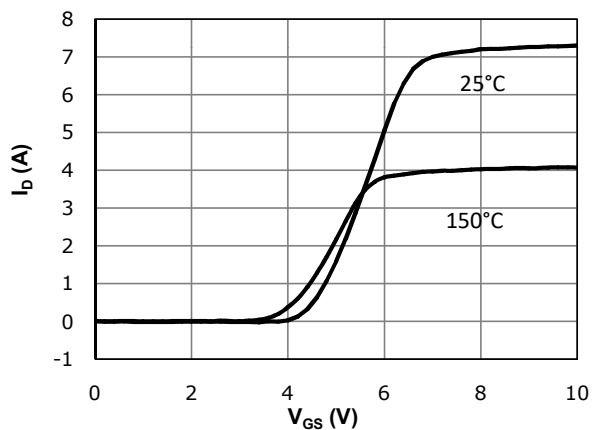


Fig 4: V_{TH} vs. T_J Temperature Characteristics

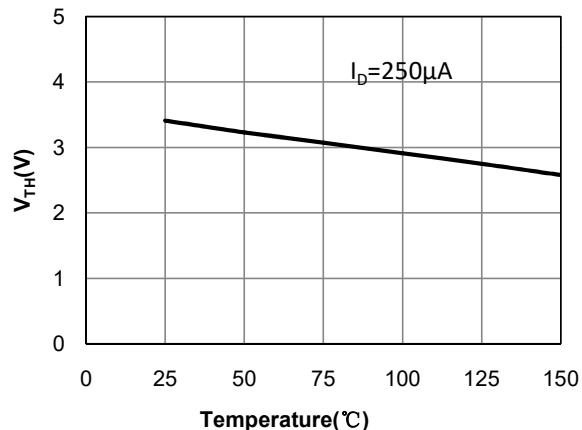


Fig 5: $R_{DS(on)}$ vs. I_{DS} Characteristics ($T_J=25^\circ\text{C}$)

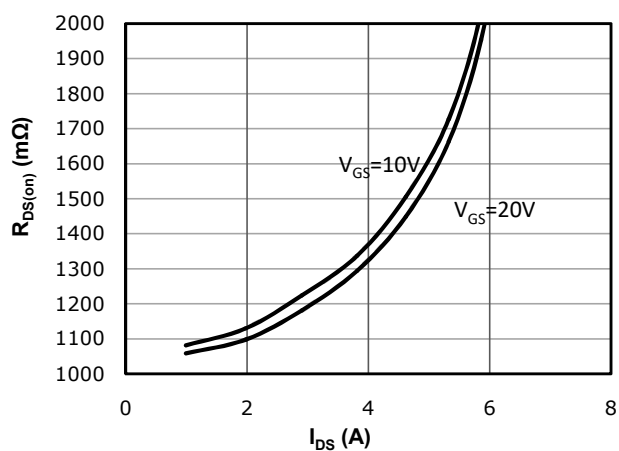


Fig 6: $R_{DS(on)}$ vs. Temperature

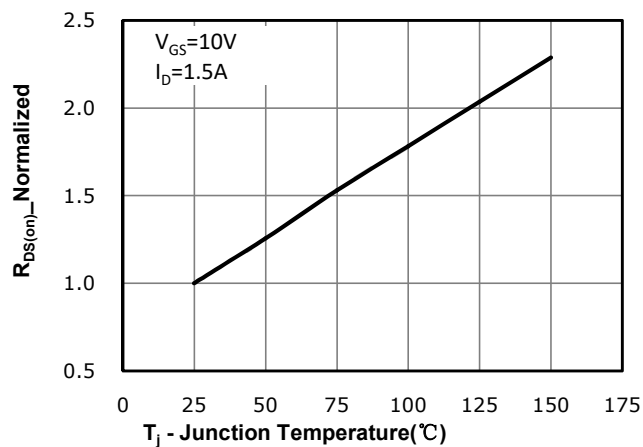


Fig 7: BV_{DSS} vs. Temperature

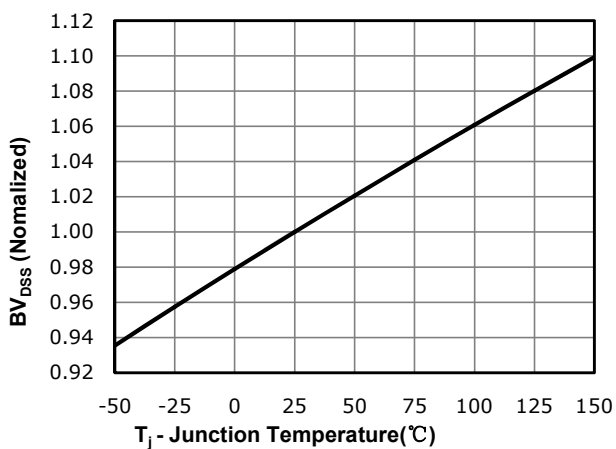


Fig 8: $R_{DS(on)}$ vs. Gate Voltage

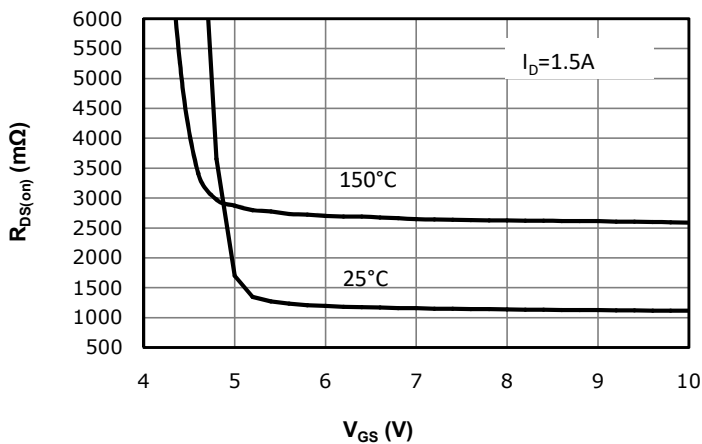


Fig 9: Body-diode Forward Characteristics

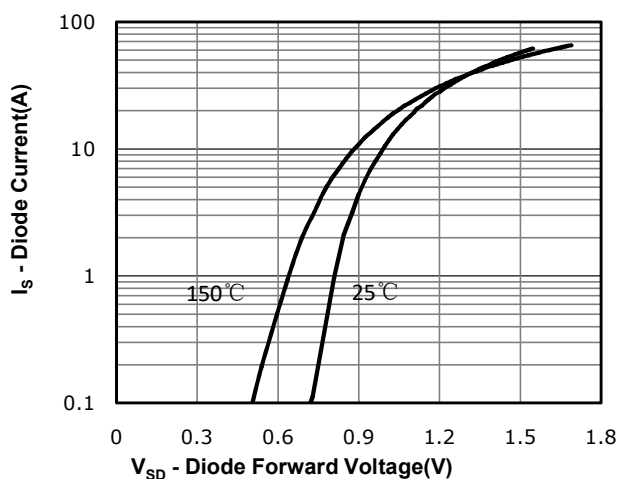


Fig 10: Gate Charge Characteristics

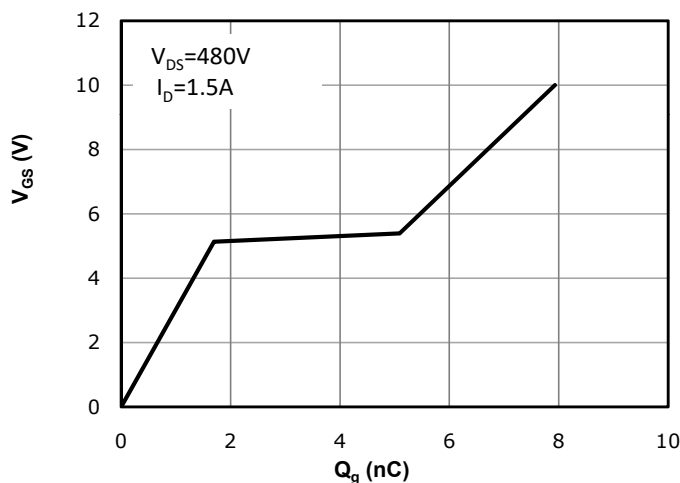


Fig 11: Capacitance Characteristics

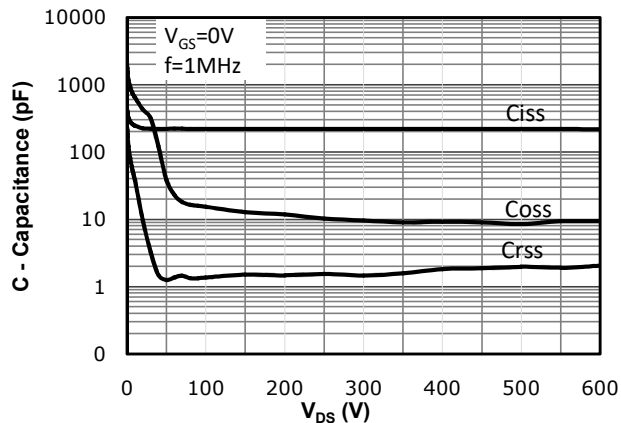


Fig 12: Safe Operating Area

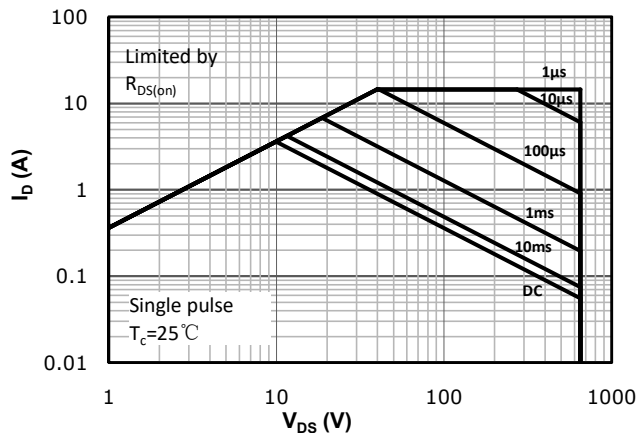
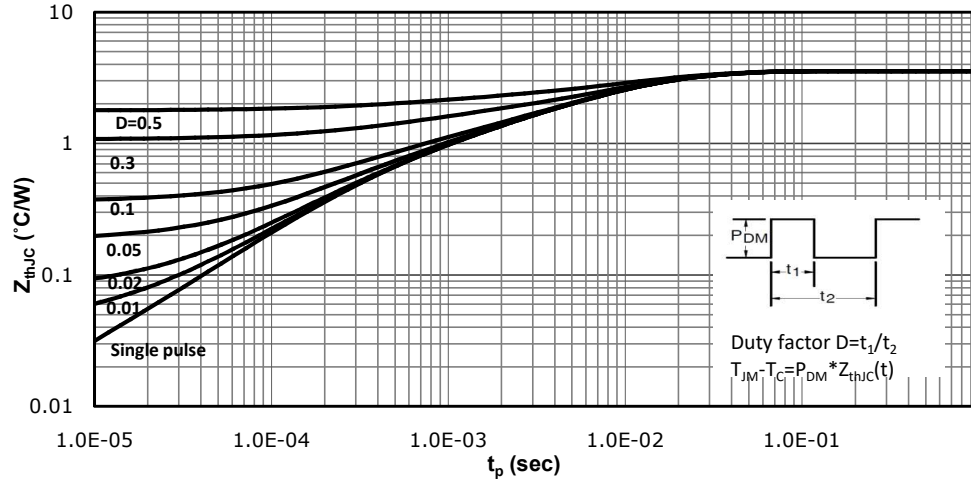
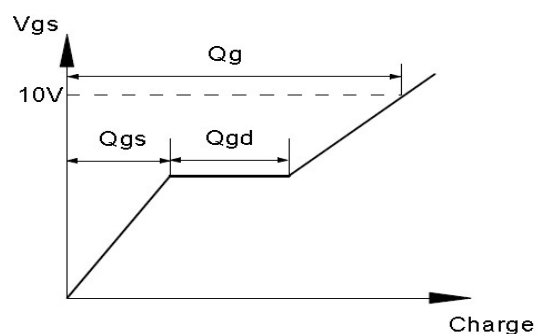
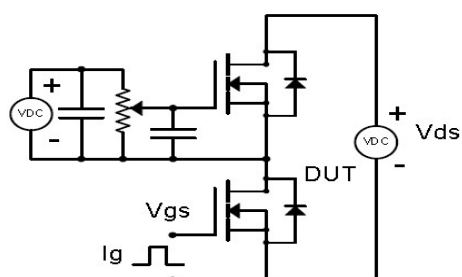


Fig 13: Max. Transient Thermal Impedance

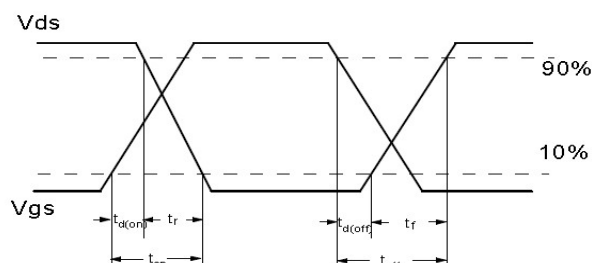
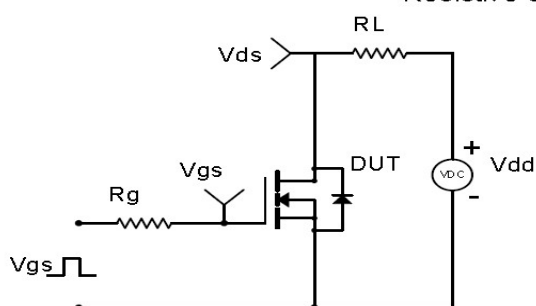


Test Circuit & Waveform

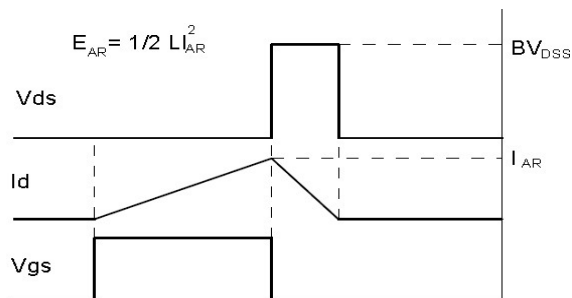
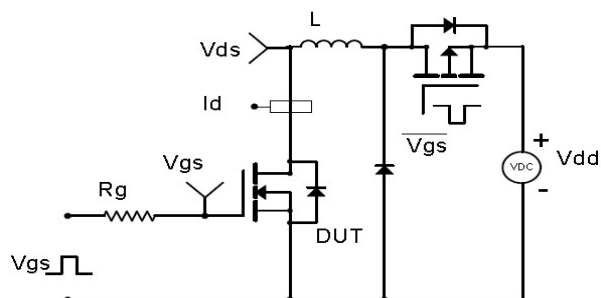
Gate Charge Test Circuit & Waveform



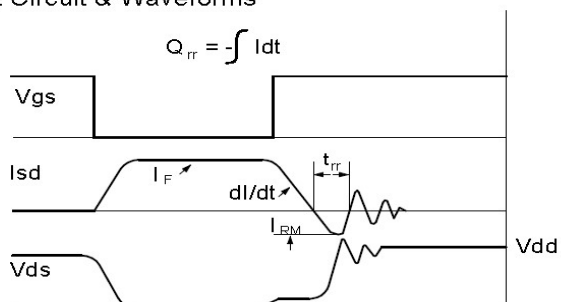
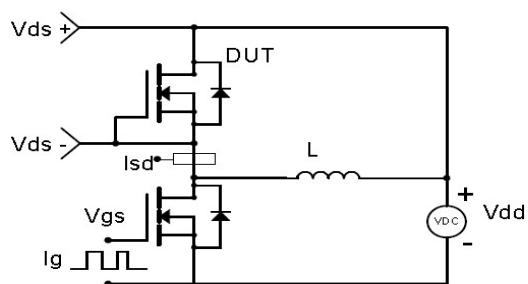
Resistive Switching Test Circuit & Waveforms



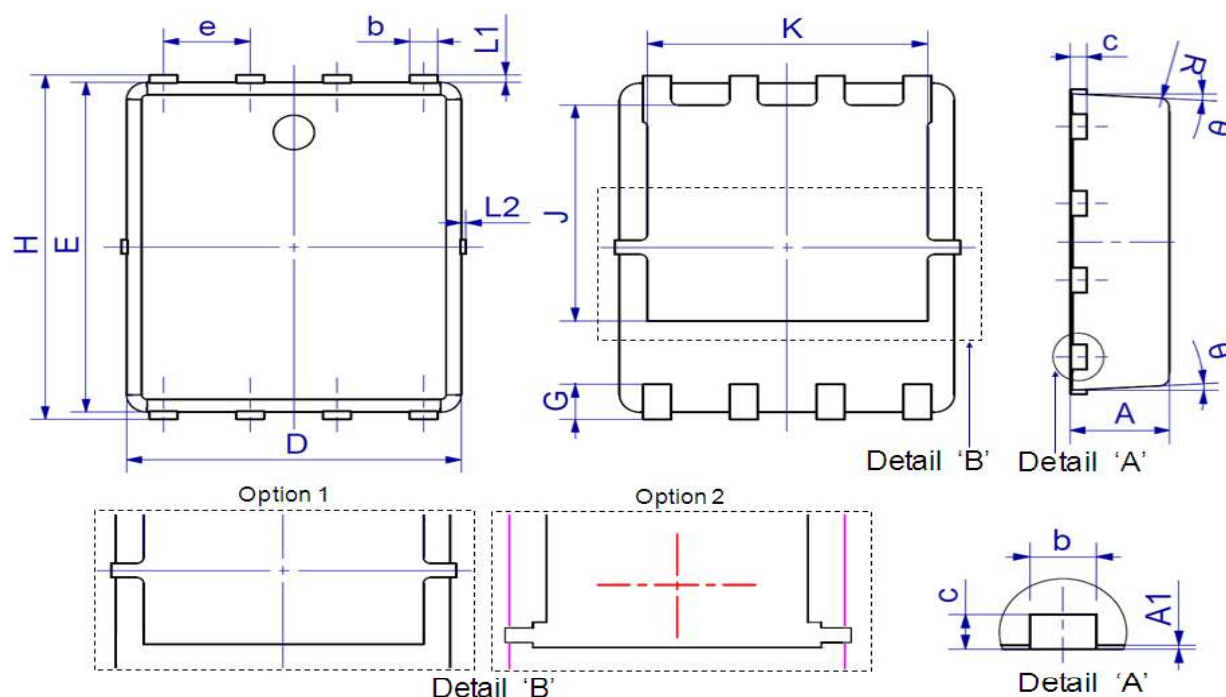
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Package Outline: DFN5*6



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.80	1.20	0.031	0.047
A1	0.00	0.05	0.000	0.002
b	0.30	0.51	0.012	0.020
c	0.15	0.35	0.006	0.014
D	4.80	5.40	0.189	0.213
e	1.27 BSC		0.050 BSC	
E	5.66	6.06	0.223	0.239
G	0.30	0.71	0.012	0.028
H	5.90	6.35	0.232	0.250
J	3.32	3.92	0.131	0.154
K	3.61	4.25	0.142	0.167
L1	0.05	0.25	0.002	0.010
L2	0.00	0.15	0.000	0.006
R	0.25 REF		0.010 REF	
θ	0°	12°	0°	12°

Marking:**NOTE:**

NXBBAAAA

N —WB code (Usually omitted)

X —Assembly location code

BB —Fab code

AAAA —Lot code

Revision History

Revision	Date	Major changes
1.2	2023/7/5	Update Datasheet Template
1.3	2023/11/13	Update V_{SD} Spec
2.0	2023/12/15	Frozen

Disclaimer

Unless otherwise specified in the datasheet, the product is designed and qualified as a standard commercial product and is not intended for use in applications that require extraordinary levels of quality and reliability, such as automotive, aviation/aerospace and life-support devices or systems.

Any and all semiconductor products have certain probability to fail or malfunction, which may result in personal injury, death or property damage. Customer are solely responsible for providing adequate safe measures when design their systems.

CRM(CQ) reserves the right to improve product design, function and reliability without notice.