Features

- Uses CRM(CQ) advanced SkyMOS2 technology
- Extremely low on-resistance $R_{DS(on)}$
- Excellent Q_gx$R_{DS(on)}$ product(FOM)
- Qualified according to JEDEC criteria

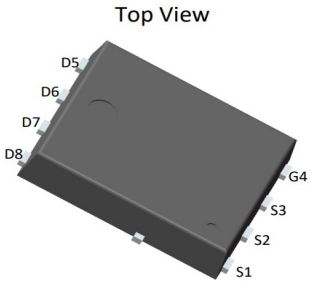
Product Summary

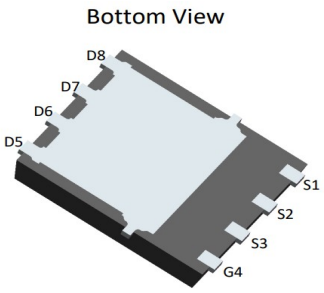
V_{DS}	40V
$R_{DS(on).typ}$	0.57mΩ
I_D	420A

100% DVDS Tested
100% Avalanche Tested

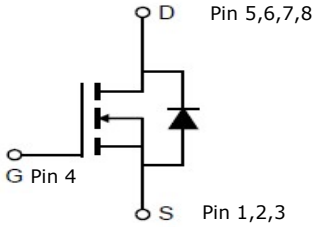
Applications

- Motor control and drive
- Battery management System
- UPS (Uninterrupible Power Supplies)





CRSM008N04L2



Package Marking and Ordering Information

Part #	Marking	Package	Packing	Reel Size	Tape Width	Qty
CRSM008N04L2	008N04L2	PDFN5x6	tape	N/A	N/A	N/A

Absolute Maximum Ratings

Parameter	**Symbol**	**Value**	**Unit**
Drain-source voltage	V_{DS}	40	V
Continuous drain current T_C = 25°C (Silicon limit) T_C = 100°C (Silicon limit)	I_D	 420 267	A
Pulsed drain current (T_C = 25°C, t_p limited by T_{jmax})	$I_{D\ pulse}$	900	A
Avalanche energy, single pulse (ID = 58A, Rg=25Ω)[1]	E_{AS}	850	mJ
Gate-Source voltage	V_{GS}	±20	V
Power dissipation (T_C = 25°C)	P_{tot}	205	W
Operating junction and storage temperature	T_j , T_{stg}	-55...+150	°C
Soldering temperature, wave soldering only allowed at leads (1.6mm from case for 10s)	Tsold	260	°C

※. Notes:
1.EAS is tested at starting Tj = 25℃, L = 0.5mH, IAS =58A, VGS = 10V.

Thermal Resistance

Parameter	Symbol	Max	Unit
Thermal resistance, junction – case.	R_{thJC}	0.61	°C/W
Thermal resistance, junction – ambient(min. footprint)	R_{thJA}	62	

Electrical Characteristic (at Tj = 25 °C, unless otherwise specified)

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Static Characteristic						
Drain-source breakdown voltage	BV_{DSS}	40	48	-	V	V_{GS}=0V, I_D=250uA
		40	48	-	V	V_{GS}=0V, I_D=1mA
Gate threshold voltage	$V_{GS(th)}$	1.2	1.7	2.2	V	V_{DS}=V_{GS},I_D=250uA
Zero gate voltage drain current	I_{DSS}	- -	- -	1 100	μA	V_{DS}=40V,V_{GS}=0V T_j=25°C T_j=125°C
Gate-source leakage current	I_{GSS}	0	-	±100	nA	V_{GS}=±20V,V_{DS}=0V
Drain-source on-state resistance	Ron	- -	0.57 0.85	0.71 1.1		VGS=10V, ID=75A VGS=4.5V, ID=75A
Transconductance	g_{fs}	-	600	-	S	V_{DS}=15V, I_D=50A
Dynamic Characteristic						
Input Capacitance	C_{iss}	-	8070	-	pF	V_{GS}=0V, V_{DS}=20V, f=1MHz
Output Capacitance	C_{oss}	-	4700	-		
Reverse Transfer Capacitance	C_{rss}	-	152	-		
Gate Total Charge	Q_G	-	140.9	-	nC	V_{GS}=10V, V_{DS}=20V, I_D=90A
Gate-Source charge	Q_{gs}	-	33.5	-		
Gate-Drain charge	Q_{gd}	-	24.4	-		
Turn-on delay time	$t_{d(on)}$	-	43.2	-	ns	V_{GS}=4.5V, V_{DD}=20V, R_{G_ext}=2.7Ω
Rise time	t_r	-	110.0	-		
Turn-off delay time	$t_{d(off)}$	-	77.8	-		
Fall time	t_f	-	81.6	-		
Gate resistance	R_G	-	2.6	-	Ω	V_{GS}=0V, V_{DS}=0V, f=1MHz

Body Diode Characteristic

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Body Diode Forward Voltage	V_{SD}	-	0.8	1.4	V	V_{GS}=0V,I_{SD}=75A
Body Diode Reverse Recovery Time	t_{rr}	-	93	-	ns	I_F=40A,dI/dt=100A/μs
Body Diode Reverse Recovery Charge	Q_{rr}	-	138	-	nC	

Typical Performance Characteristics

Fig 1: Output Characteristics

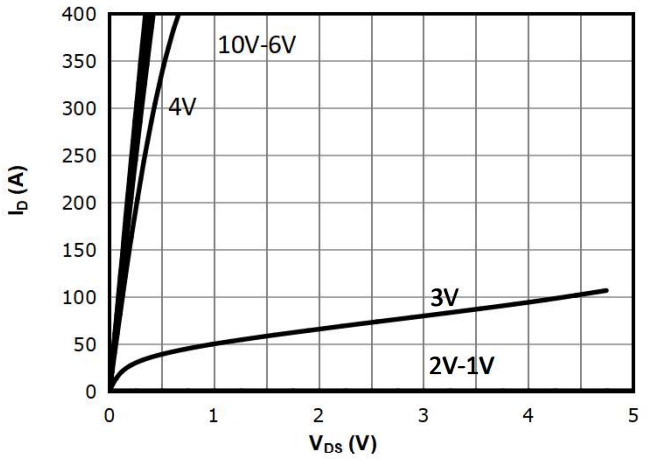


Fig 2: Transfer Characteristics

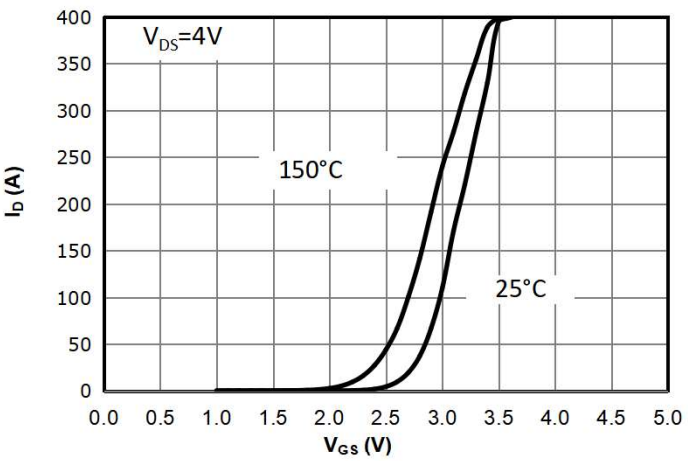


Fig 3: Rds(on) vs Drain Current and Gate Voltage

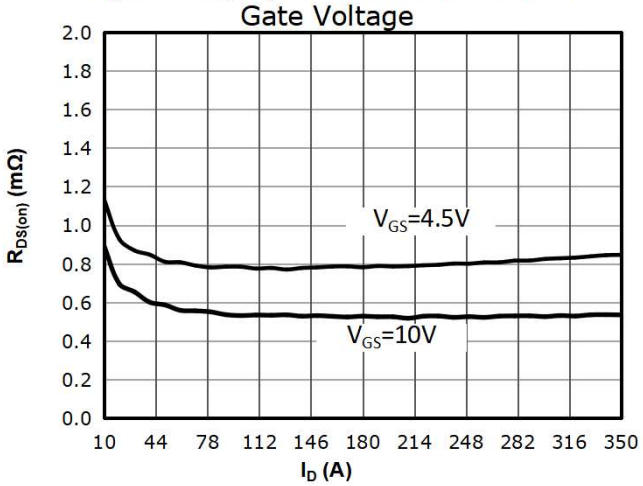


Fig 4: Rds(on) vs Gate Voltage

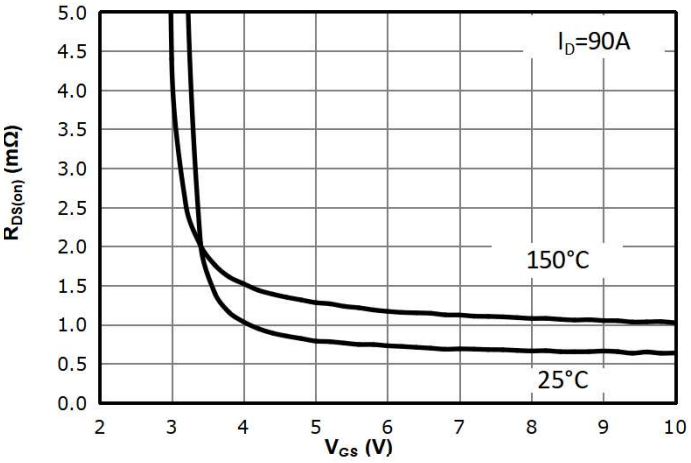


Fig 5: Rds(on) vs. Temperature

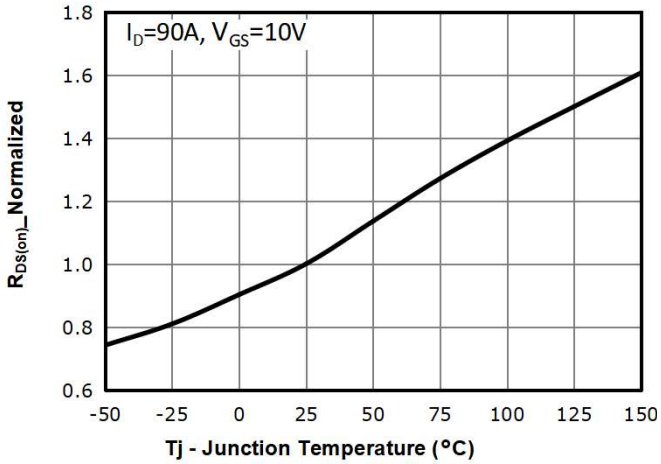


Fig 6: Vgs(th) vs. Temperature

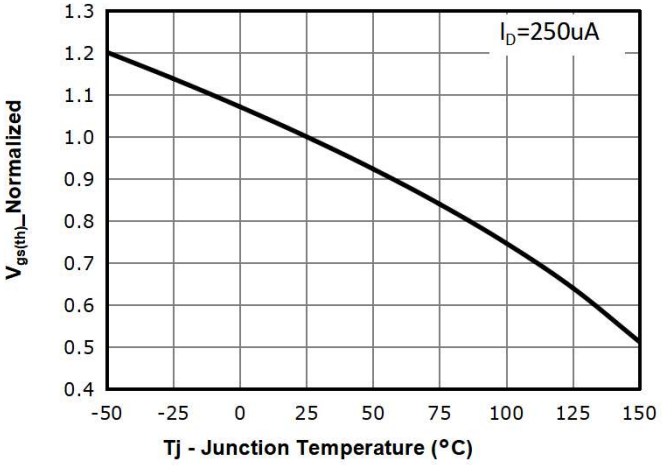


Fig 7: BVdss vs. Temperature

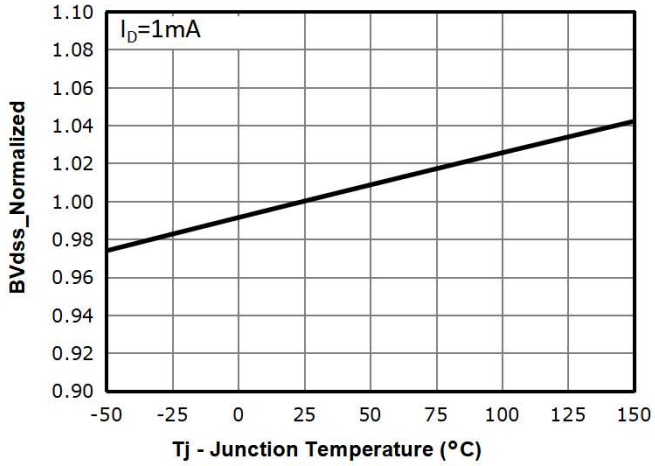


Fig 8: Capacitance Characteristics

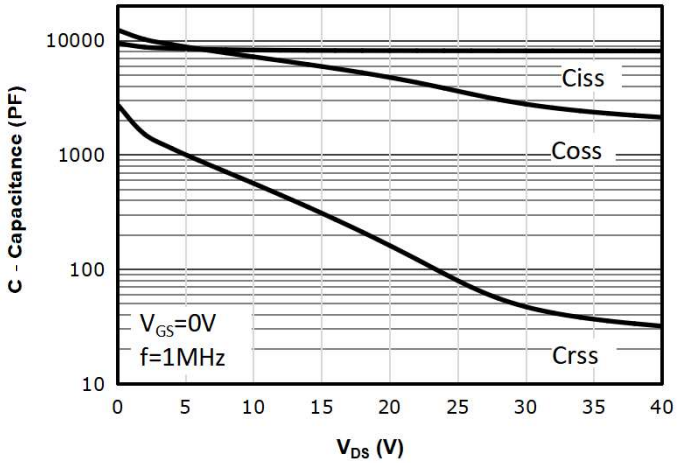


Fig 9: Gate Charge Characteristics

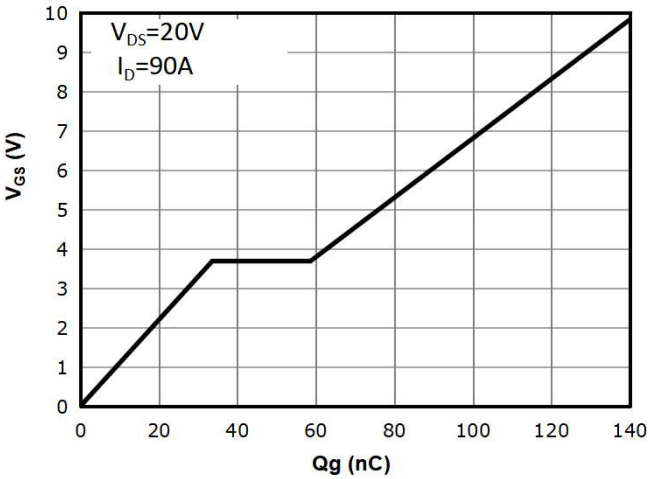


Fig 10: Body-diode Forward Characteristics

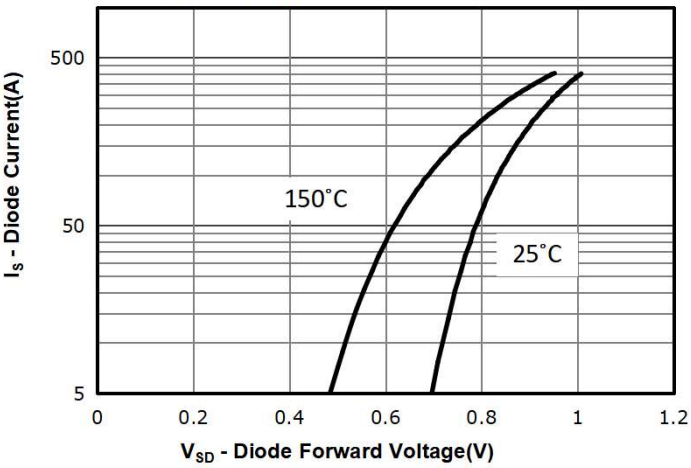


Fig 11: Power Dissipation

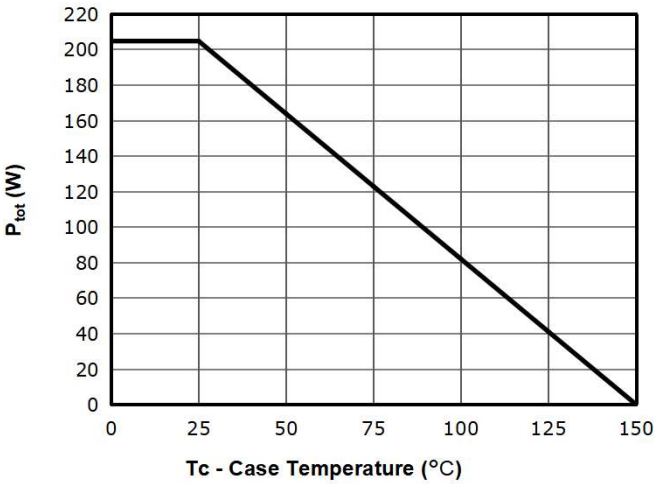


Fig 12: Drain Current Derating

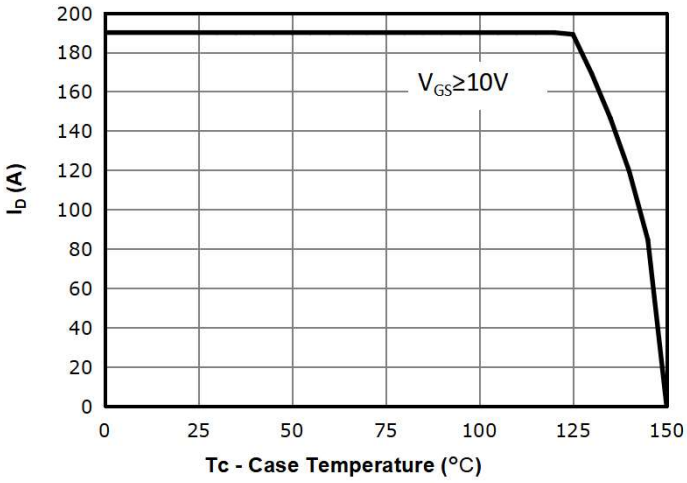


Fig 13: Safe Operating Area

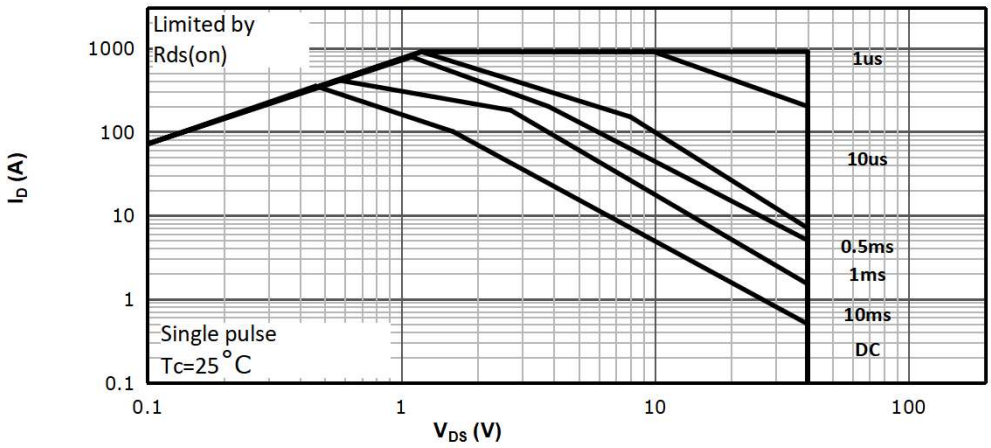
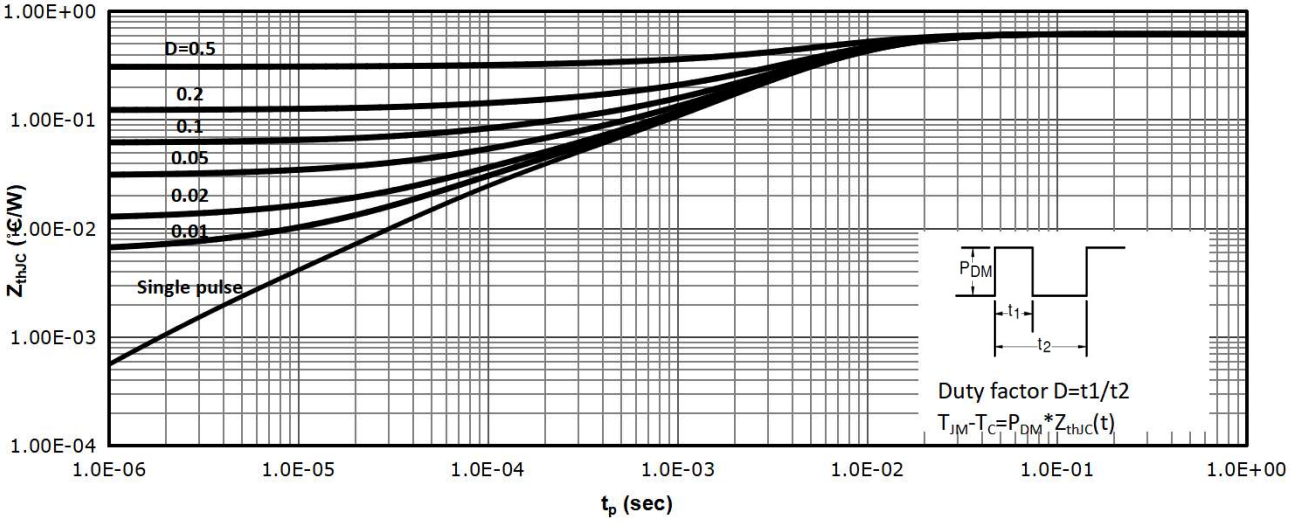
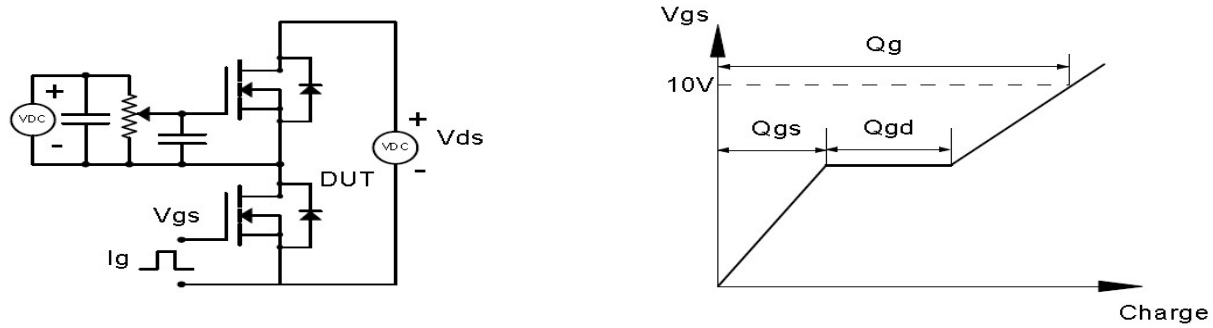


Fig 14: Max. Transient Thermal Impedance

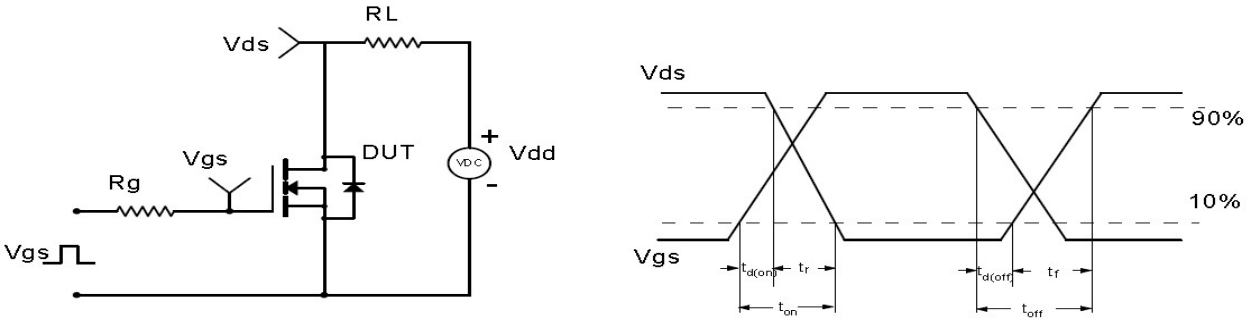


Test Circuit & Waveform

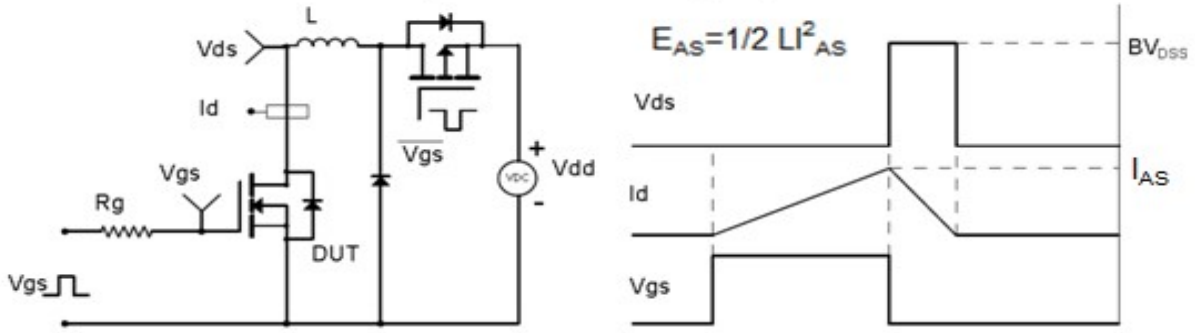
Gate Charge Test Circuit & Waveform



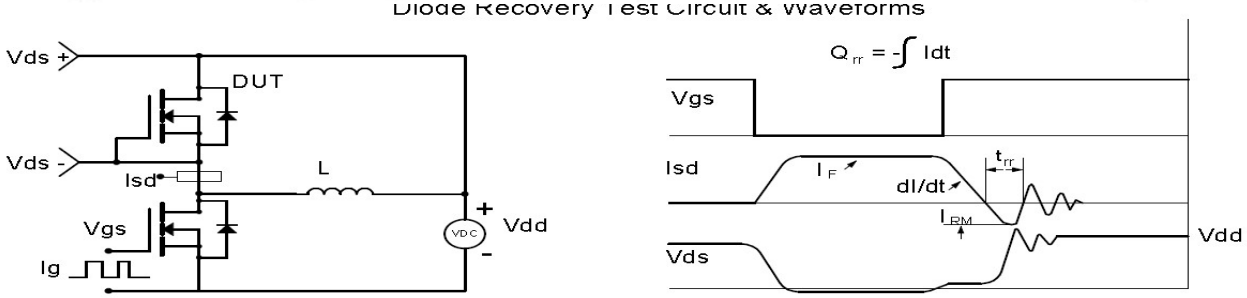
Resistive Switching Test Circuit & Waveforms



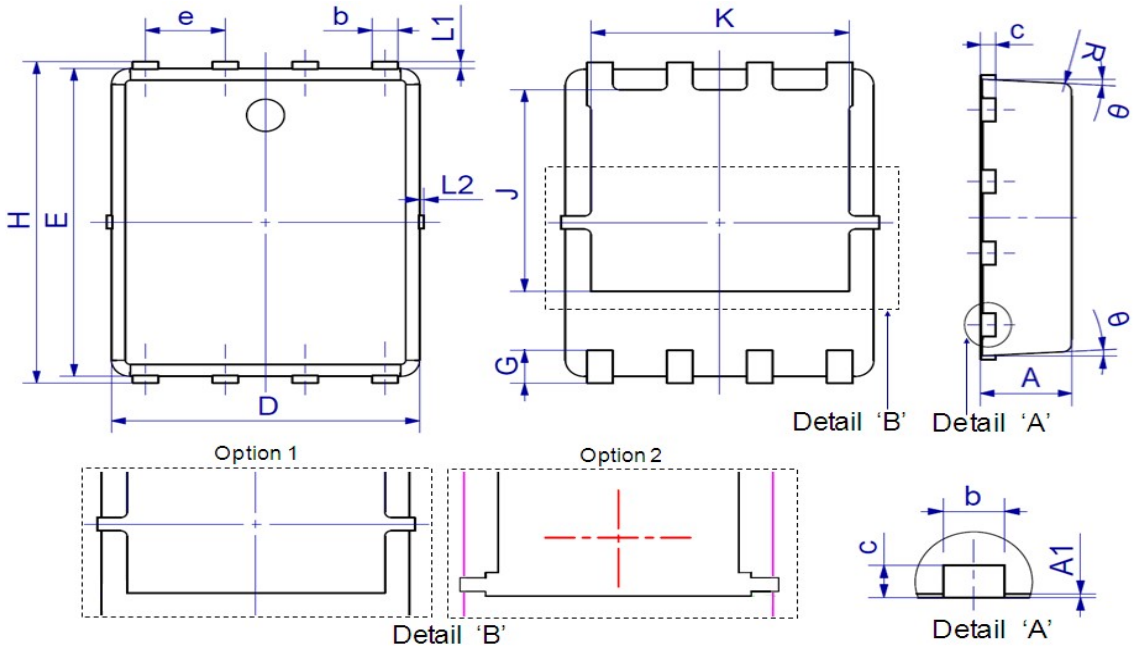
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

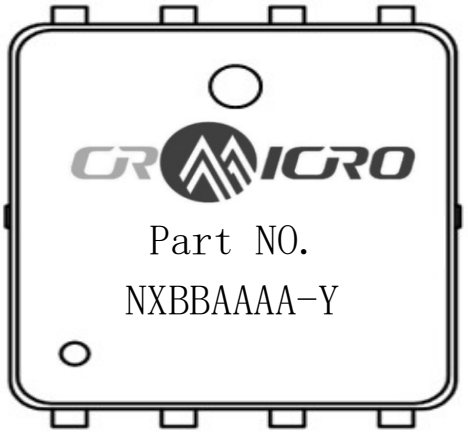


Package Outline: PDFN5x6



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.80	1.20	0.031	0.047
A1	0.00	0.05	0.000	0.002
b	0.30	0.51	0.012	0.020
c	0.15	0.35	0.006	0.014
D	4.80	5.40	0.189	0.213
e	1.27 BSC		0.050 BSC	
E	5.66	6.06	0.223	0.239
G	0.30	0.71	0.012	0.028
H	5.90	6.35	0.232	0.250
J	3.32	3.92	0.131	0.154
K	3.61	4.25	0.142	0.167
L1	0.05	0.25	0.002	0.010
L2	0.00	0.15	0.000	0.006
R	0.25 REF		0.010 REF	
θ	0°	12°	0°	12°

Marking



NOTE:
NXBBAAAAY

N	—Wire Bond code
X	—Assembly location code
BB	—Fab code
AAAA	—Lot code
Y	—Bin code

Revision History

Revision	Date	Major changes
1.0	2025/6/29	Release of Preliminary version.
1.1	2025/9/9	update Trr Qrr and SOA.

Disclaimer

Unless otherwise specified in the datasheet, the product is designed and qualified as a standard commercial product and is not intended for use in applications that require extraordinary levels of quality and reliability, such as automotive, aviation/aerospace and life-support devices or systems.

Any and all semiconductor products have certain probability to fail or malfunction, which may result in personal injury, death or property damage. Customer are solely responsible for providing adequate safe measures when design their systems.

CRM(CQ) reserves the right to improve product design, function and reliability without notice.