

Features

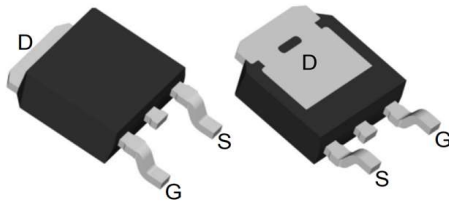
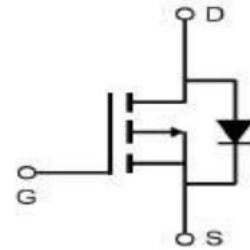
- Uses CRM(CQ) advanced Trench technology
- Extremely low on-resistance $R_{DS(on)}$
- Excellent $Q_g \times R_{DS(on)}$ product(FOM)
- AEC-Q101 Qualified
- MSL1 up to 260°C peak reflow

Applications

- Motor control and drive
- Battery management
- UPS (Uninterruptible Power Supplies)

Product Summary

V_{DS}	-60V
$R_{DS(on)}$ @10V typ	9.2mΩ
I_D	-72A

100% DVDS Tested
100% Avalanche Tested

CRTD125P06LQ

Package Marking and Ordering Information

Part #	Marking	Package	Packing	Reel Size	Tape Width	Qty
CRTD125P06LQ	125P06LQ	TO-252	Tape&reel	N/A	N/A	2500pcs

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	-60	V
Continuous drain current $T_C = 25^\circ\text{C}$ (Silicon limit) $T_C = 25^\circ\text{C}$ (Package limit) $T_C = 100^\circ\text{C}$ (Silicon limit)	I_D	-72 -90 -51	A
Pulsed drain current ($T_C = 25^\circ\text{C}$, t_p limited by T_{jmax})	$I_{D \text{ pulse}}$	-289	A
Avalanche energy, single pulse ($I_D = -30\text{A}$, $R_g = 25\Omega$) ^[1]	E_{AS}	225	mJ
Gate-Source voltage	V_{GS}	± 20	V
Power dissipation ($T_C = 25^\circ\text{C}$)	P_{tot}	135	W
Operating junction and storage temperature	T_j, T_{stg}	-55...+175	$^\circ\text{C}$
Soldering temperature, wave soldering only allowed at leads (1.6mm from case for 10s)	T_{sold}	260	$^\circ\text{C}$

Notes:1.EAS was tested at $T_j = 25^\circ\text{C}$, $L = 0.5\text{mH}$, $I_{AS} = -30\text{A}$, $V_{gs} = -10\text{V}$.

Thermal Resistance

Parameter	Symbol	Max	Unit
Thermal resistance, junction – case (junction-heat-spreader)	R_{thJC}	1.11	$^\circ\text{C/W}$
Thermal resistance, junction – ambient(min. footprint)	R_{thJA}	62	
Thermal resistance, junction – plastic case	R_{thJ-pc}	34	

Electrical Characteristic (at T_j = 25 °C, unless otherwise specified)

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Static Characteristic						
Drain-source breakdown voltage	BV _{DSS}	-60	-	-	V	V _{GS} =0V, I _D =-250uA
		-60	-	-	V	V _{GS} =0V, I _D =-1mA
Gate threshold voltage	V _{GS(th)}	-1	-	-2.5	V	V _{DS} =V _{GS} , I _D =-250uA
Zero gate voltage drain current	I _{DSS}	-	-	-1	μA	V _{DS} =-60V, V _{GS} =0V
		-	-	-100		T _j =25°C T _j =125°C
Gate-source leakage current	I _{GSS}	-	-	±100	nA	V _{GS} =±20V, V _{DS} =0V
Drain-source on-state resistance	R _{DS(on)}	-	9.2	12.5	mΩ	V _{GS} =-10V, I _D =-30A
			11.7	21		V _{GS} =-4.5V, I _D =-24A
Transconductance	g _{fs}	26	52	104	S	V _{DS} =-5V, I _D =-25A

Dynamic Characteristic

Input Capacitance	C _{iss}	3518	7035	14070	pF	V _{GS} =0V, V _{DS} =-30V, f=1MHz
Output Capacitance	C _{oss}	84	421	2105		
Reverse Transfer Capacitance	C _{rss}	68	341	1705		
Gate Total Charge	Q _G	66	133	265	nC	V _{GS} =-10V, V _{DS} =-30V, I _D =-25A, f=1MHz
Gate-Source charge	Q _{gs}	13	27	54		
Gate-Drain charge	Q _{gd}	12	25	49		
Turn-on delay time	t _{d(on)}	12	24	47	ns	V _{GS} =-10V, V _{DS} =-30V, R _{G_ext} =3Ω, I _D =-25A
Rise time	t _r	44	87	175		
Turn-off delay time	t _{d(off)}	47	94	188		
Fall time	t _f	54	109	217		
Gate resistance	R _G	-	1.73	8	Ω	V _{GS} =0V, V _{DS} =0V, f=1MHz

Body Diode Characteristic

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Body Diode Forward Voltage	V _{SD}	-	-0.8	-1.3	V	V _{GS} =0V, I _{SD} =-30A
Body Diode Reverse Recovery Time	t _{rr}	15	31	61	ns	I _F =-25A, dI/dt=100A/μs
Body Diode Reverse Recovery Charge	Q _{rr}	10	20	39	nC	

Typical Performance Characteristics

Fig 1: Output Characteristics

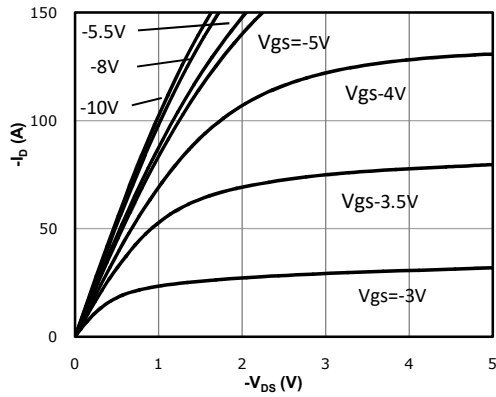


Fig 2: Transfer Characteristics

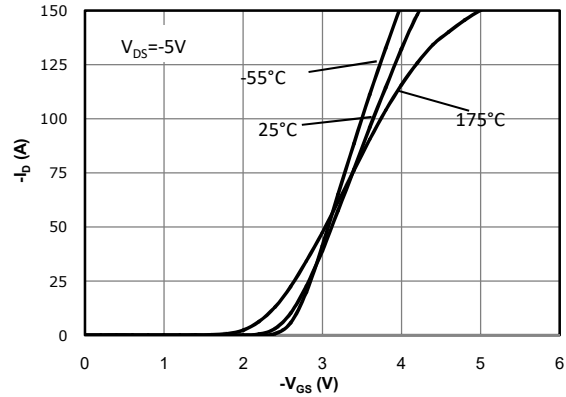
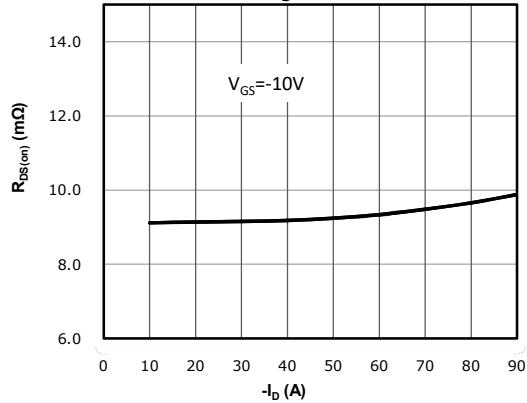
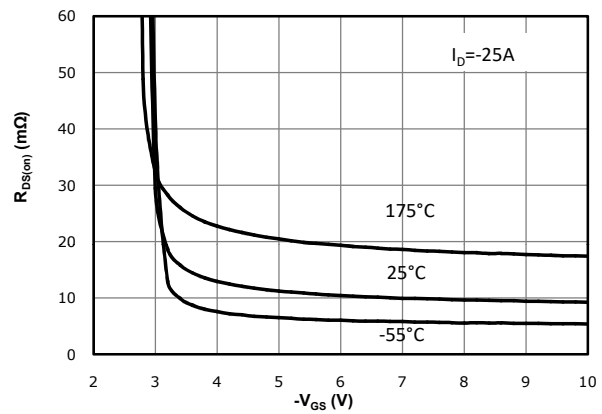
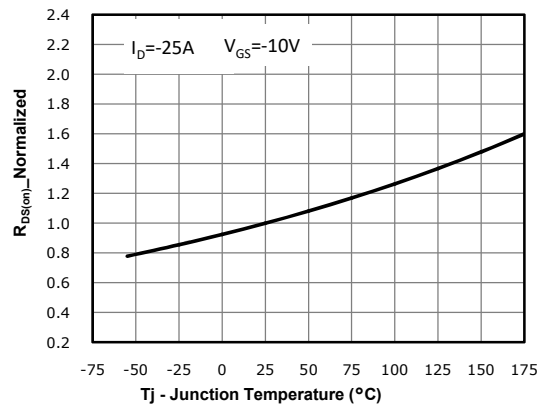
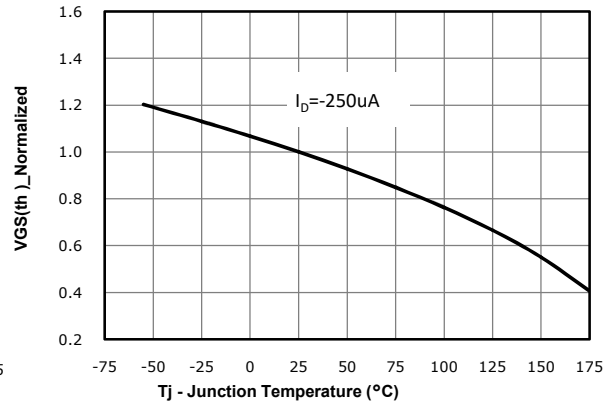

Fig 3: $R_{DS(on)}$ vs Drain Current and Gate Voltage

Fig 4: $R_{DS(on)}$ vs Gate Voltage

Fig 5: $R_{DS(on)}$ vs. Temperature

Fig 6: $V_{GS(th)}$ vs. Temperature


Fig 7: BVds vs. Temperature

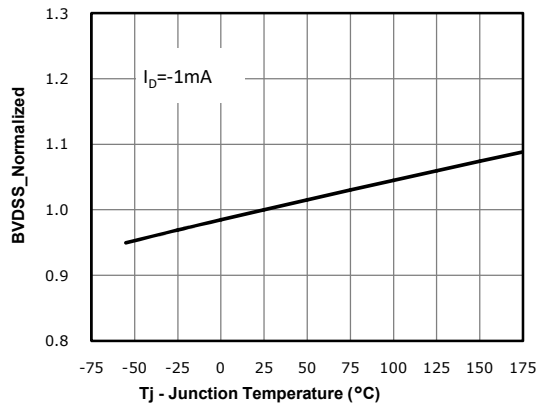


Fig 8: Capacitance Characteristics

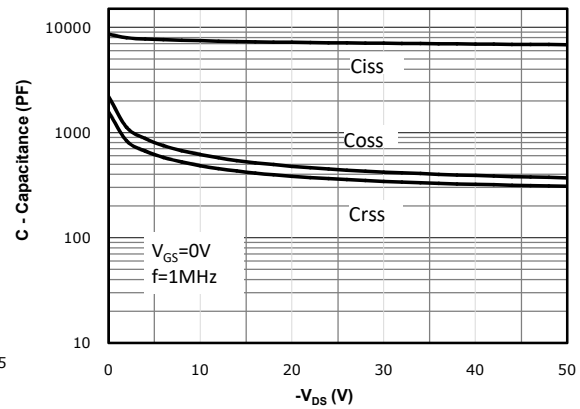


Fig 9: Gate Charge Characteristics

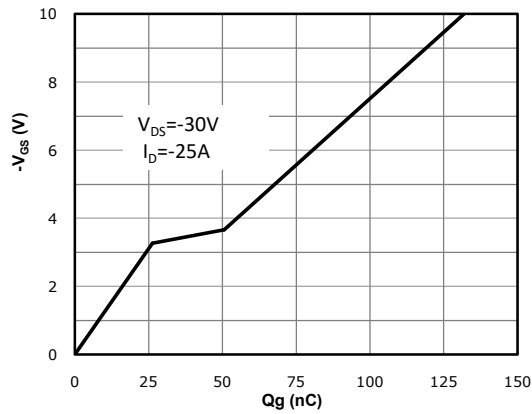


Fig 10: Body-diode Forward Characteristics

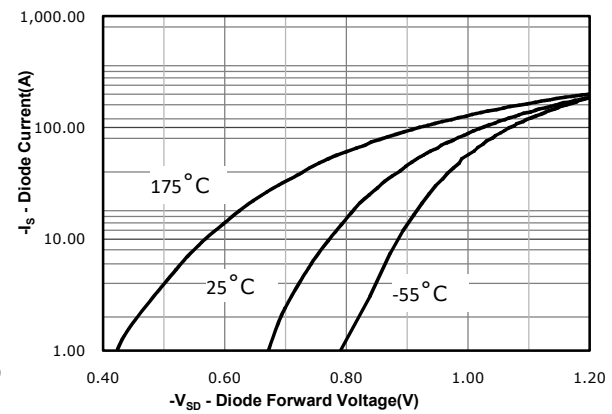


Fig 11: Power Dissipation

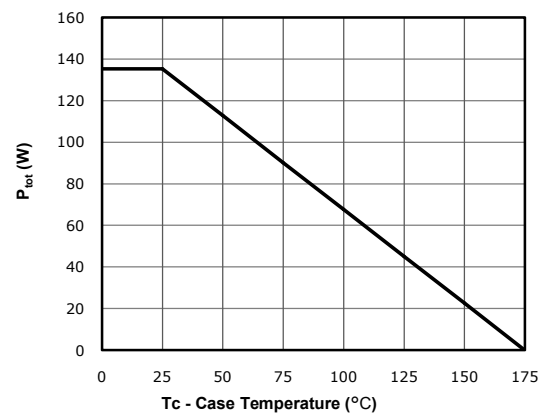


Fig 12: Drain Current Derating

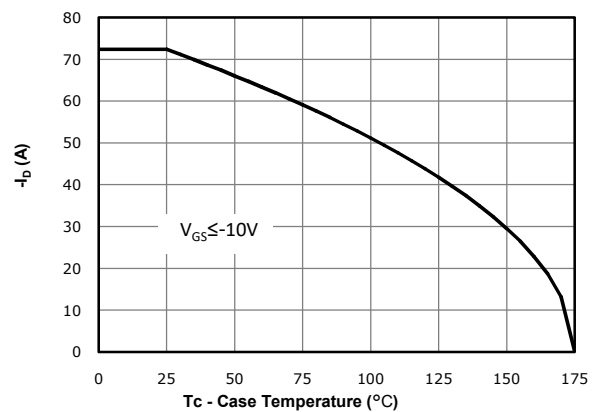


Fig 13: Safe Operating Area

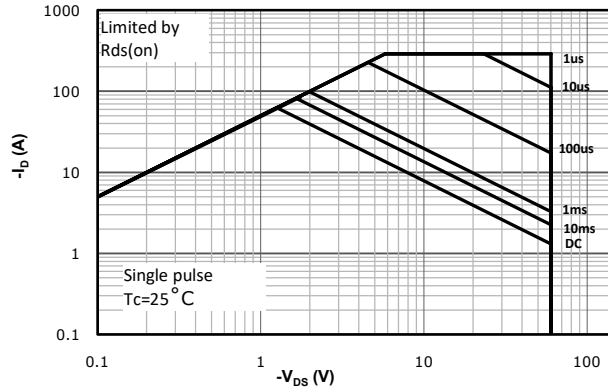
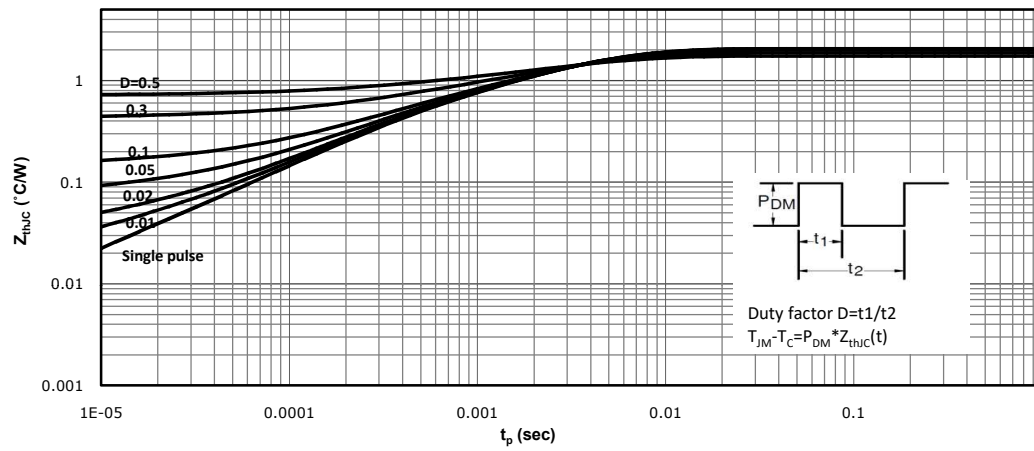
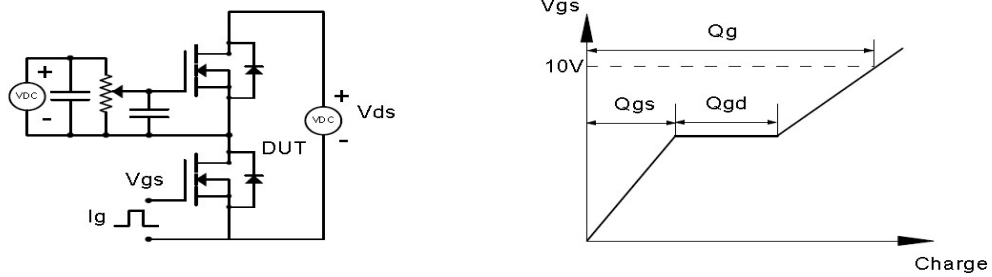


Fig 14: Max. Transient Thermal Impedance

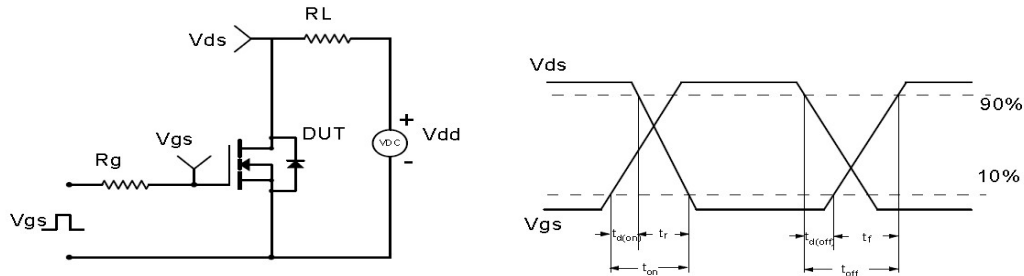


Test Circuit & Waveform

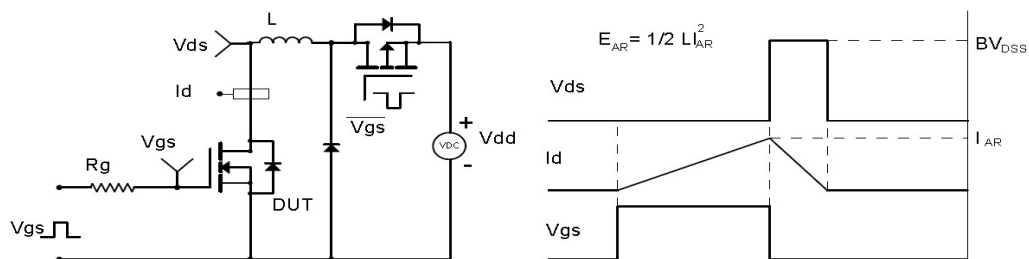
Gate Charge Test Circuit & Waveform



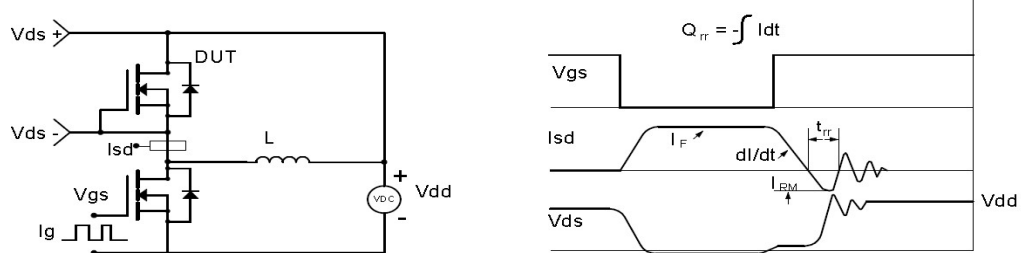
Resistive Switching Test Circuit & Waveforms



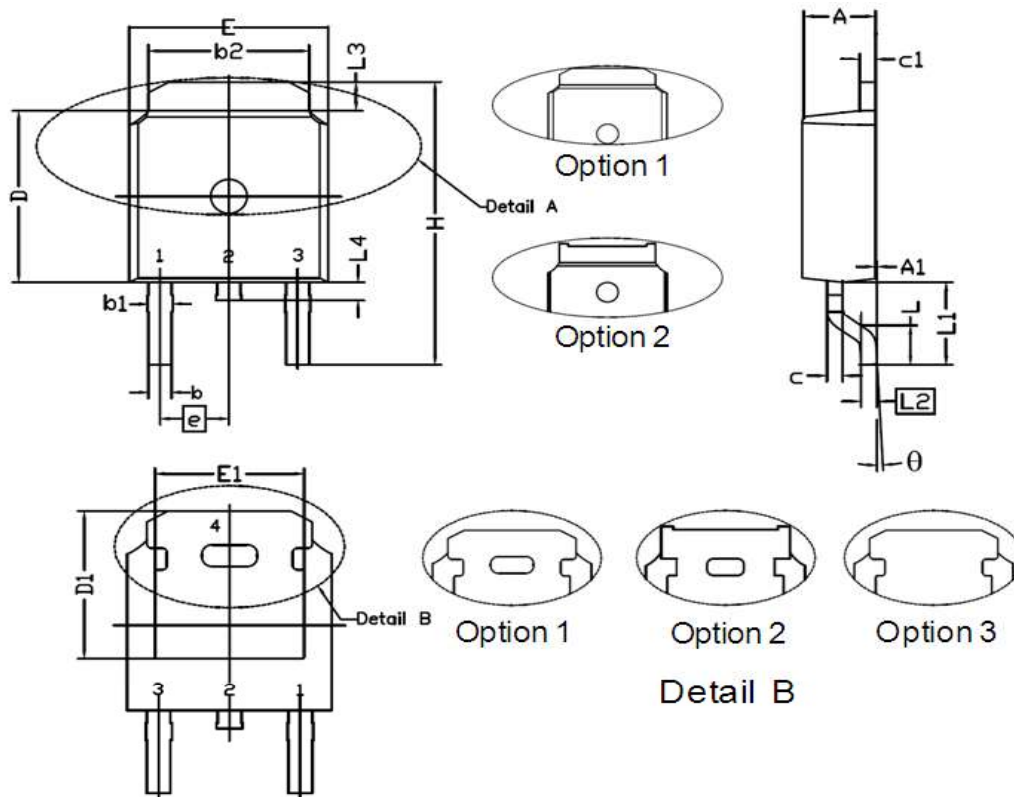
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Package Outline: TO-252



Symbol	Dimensions In Millimeters		
	Min.	Nom.	Max.
A	2.15	2.30	2.38
A1	0.00	0.07	0.15
b	0.60	0.76	0.91
b1	0.65	--	1.15
b2	5.00	5.33	5.50
c	0.45	0.50	0.61
c1	0.36	0.50	0.66
D	5.80	6.10	6.22
D1	5.21	5.25	5.65
e	2.29 BSC.		
E	6.30	6.50	6.65
E1	4.75	5.10	5.45
H	9.40	9.90	10.40
L	1.38	1.52	1.78
L1	2.92 REF		
L2	0.508 BSC.		
L3	0.72	1.01	1.35
L4	0.60	0.75	1.20
θ	0°	--	8°

Marking**NOTE:**

XAAAAAAAA-Y

X

—Assembly location code

AAAAAAA

—Assembly lot NO. last 7 digits

Y

—Bin code

Revision History

Revision	Date	Major changes
1.0	2023/8/24	Release of preliminary 1.0 version.
1.1	2023/11/10	Update POD 尺寸
1.2	2024/1/11	Update VTH SPEC

Disclaimer

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